In re Patent Application of
MARINET ET AL.
Serial No. **09/995,258**
Filed: **NOVEMBER 27, 2001**

In the Specification:

Please replace the paragraphs recited at page 9, lines 10-34 with the following rewritten paragraphs:

Channel 24 as a whole is overlaid with a gate 21 composed of a thin electrically insulating layer, for example, polycrystalline silicon. The insulating layer is overlaid with a metal contact serving as the gate connection. Both ends of the channel include contacts 23, 29 connected to respective metal contacts 22, 28 providing the drain and the source of the transistor, respectively.

The drain-source current includes a random component when the channel dimensions are chosen to be close to the minimum resolution allowed by the manufacturing technology in use. The dimensions may even be slightly less than this minimum because defects may otherwise appear when developing the channel implantation mask. Therefore, as shown in the enlarged view in FIG. 3b ~~FIG. 3a~~, when the channel 24 includes dimensions and a folding step that are close to the limits allowed by the technology in use, or even slightly smaller than these limits, the folded portions obtained include a rounded shape 24' inside the fold. For example, with a 0.35 mm integration technology, the width of parallel 25, 26 and folded portions of the gate is less than 1 mm, and preferably approximately 0.7 mm, whereas the distance between parallel portions is on the order of 1.5 mm.